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Application Note

CDIAN003

CDI GaN Bias Board User's Guide

Revision 4.0
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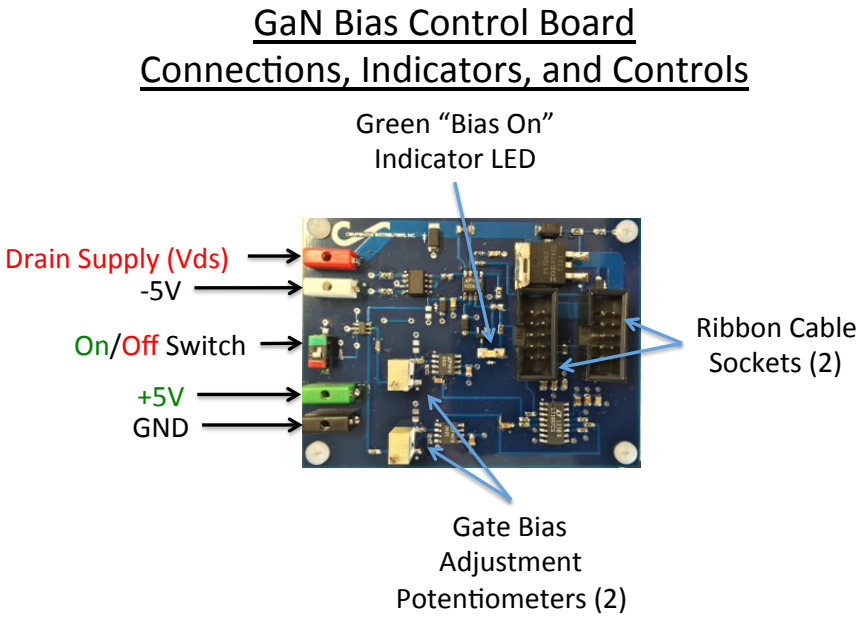
Quick Start Guide

Shown below are the essential connections, controls, and indicators for the GaN Bias Control Board.



Mating connectors for the power supply connections should be E-Z-HOOK 0.08" diameter test leads (part numbers 9259RED, 9259WTE, 9259GRN, or 9259BLK). The GaN Bias Control board provided by CDI will include a set of power supply leads and ribbon cables.

Usage procedure:

1. Connect the power supply leads (Red, White, Green, and Black) to the appropriate lab power supplies.
2. Connect power supply sense lines from Red and Black to appropriate sense pins on the lab power supply (sense lines are included in the CDI provided cable assembly).
3. Move the On/Off switch to "**off**" (Red position).
4. Turn on and adjust all lab supplies to the correct voltages. Insure that current limits are set appropriately.
5. Disconnect any ribbon cable assemblies from the target GaN device board.
6. Move the On/Off switch to "**on**" (Green position).
7. Using a multi-meter, verify that the V_{dd}, V_{g1}, and V_{g2} voltages are correct. Adjust the potentiometers to tune V_{g1} and V_{g2} as needed.
8. Move the On/Off switch to "**off**".
9. Disable the output of **all** lab supplies.
10. Connect the ribbon cable or cables to the target GaN evaluation board.
11. Enable the output of all lab supplies
12. Move the On/Off switch to "**on**" to bias on the target GaN device(s). Move it to "**off**" to remove bias from the target GaN evaluation board.

Overview

Gallium Nitride (GaN) transistors from Sumitomo Electric Device Innovations (SEDI) are depletion mode devices that require special gate and drain bias sequencing to prevent catastrophic damage to the device. This application note provides an overview of GaN device bias requirements and how to address them. This application note is written to be used in conjunction with the CDI designed "GaN Bias Board" which implements the circuits described within the application note. Please send any questions regarding this document or GaN device biasing in general to rf@cdiweb.com.

GaN FET Bias Requirements

FET transistors are three-terminal devices. The three terminals are identified as:

1. Source (S) – the terminal through which carriers enter the channel.
2. Drain (D) – the terminal through which carriers exit the channel.
3. Gate (G) – the terminal that provides control of carrier flow.

A FET transistor controls the flow of electrons (or electron holes) from the source to the drain by affecting the size of a conductive channel. Varying a voltage across the gate and source terminals controls the size of the channel.

A Sumitomo GaN FET is a depletion mode device. "Depletion mode" refers to the channel control mechanism. When a negative voltage is applied between the Gate and Source terminals, an area of carrier depletion is formed within the channel, restricting the flow of current. Without this negative voltage, the channel is fully open, and maximum current can flow from drain to source, which can quickly destroy the device through electrical over stress. As the Gate to Source bias voltage becomes more negative, the device reaches a state known a "pinch-off", where all of the drain to source current flow is restricted and the device is effectively "off".

The primary purpose of the GaN bias board is to prevent over current damage to the GaN power transistor by providing a negative Gate-Source bias voltage before a Drain-Source voltage is applied. This order is reversed with powering down the device. A secondary consideration of our application circuit is to protect against accidental over-current conditions that may occur due to circuit faults or extremely high levels of RF overdrive. The third consideration of the application circuit is to provide a safe shut-down mechanism in the case of a GaN FET device over-temperature condition.

GaN Device Bias Voltage Sequencing

Sumitomo's GaN devices are rated for 24, 28, or 48V (typical) Drain-Source voltage. The specific voltage requirement depends on the device itself. However, the basic requirements for the application circuit remain the same. For this application note a 48V drain supply voltage (V_{ds}) will be referenced for convenience.

Examining a typical Sumitomo GaN device datasheet (EGNB045MK), the Gate-Source pinch-off voltage (V_{gs}) is defined with the following specifications:

Minimum = -1.0V
Typical = -2.0V
Maximum = -3.5V

Therefore, the circuit will provide at least a -4.0V Gate-Source voltage (V_{gs}) to assure pinch-off before V_{ds} (48V in this example) is applied.

Figure 1 shows the three voltages sequenced for a two stage 20W GaN amplifier. The initial "**off**" state voltages for V_{gs1} and V_{gs2} is -4.35V and V_{ds} for both stages is 0V. After the On/Off switch is moved to the "**on**" position, V_{ds} of 48V is applied to both stages. Next, after 120ms V_{gs2} is set to -1.21V. Then, after another 120ms V_{gs1} is set to -1.11V. At this point, the part is fully biased and ready for evaluation.

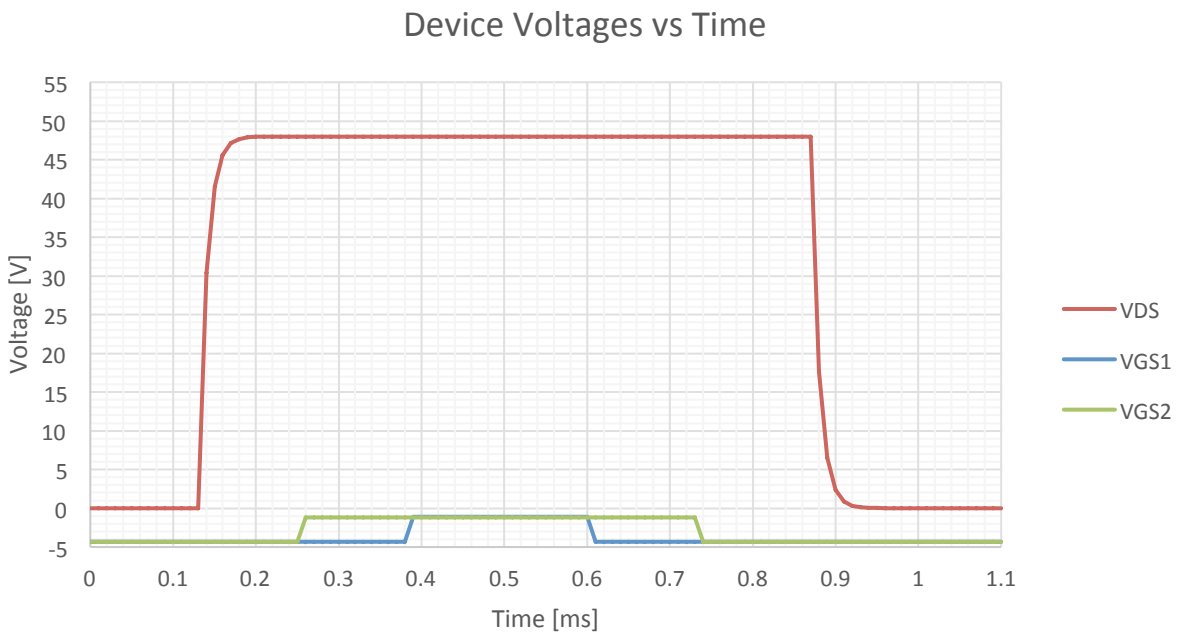


Figure 1 - Device Voltages vs Time

After RF testing is completed and input RF drive is removed, the GaN amplifier bias is disabled by moving the On/Off switch to the "**off**" position. First, V_{gs1} is set to -4.35V. Then

V_{gs2} is set to -4.35V. Last, V_{ds} for both devices is removed. It is important to maintain V_{gs} in the pinch-off region until V_{ds} has dropped to very near zero to maintain stability of the GaN device.

CDI GaN Bias Board Theory of Operation

Bias Board Connections

Figure 2 shows the I/O connections to the bias board. Refer also to the "Quick Start Guide" at the beginning of this document for an image of the assembled board.

The two 10-pin ribbon cable headers (J5 and J6) are "keyed". This ensures they cannot accidentally be connected backwards when used with the appropriate ribbon cables. Multiple pins are used for V_{dd} (V_{dd} = V_{ds}) and ground to accommodate the higher current that is expected for these signals.

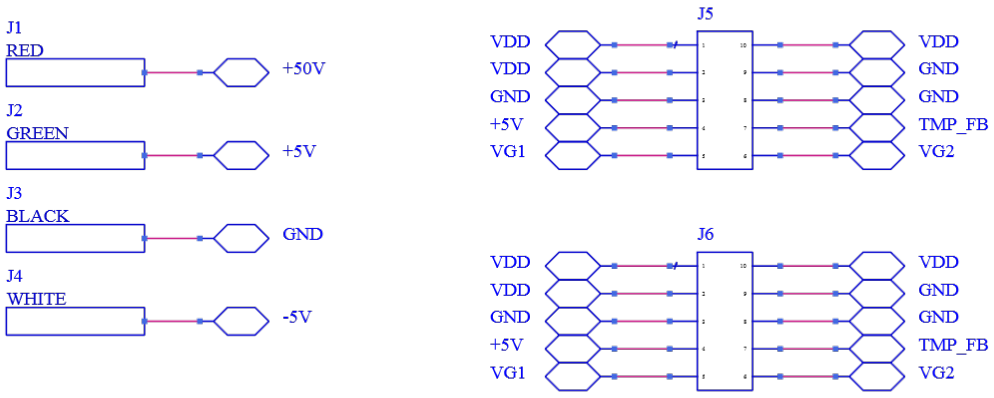


Figure 2 - Bias Board Connections

Supply Sequencing Circuit

At the heart of the application board is a sequencing IC, the Texas Instruments LM3880. The LM3880 provides three open-drain outputs (called flags) that are enabled in a specific sequence when the LM3880 logic input is enabled or disabled. The open-drain outputs are pulled low when the LM3880 is logic input is low, or when V_{CC} is not applied to the LM3880. After V_{CC} is applied to the LM3880 and the logic input is high, the open-drain flag lines allowed to "float" to a high-impedance open-drain state. Figure 3 shows the supply sequencing circuit on the bias control board.

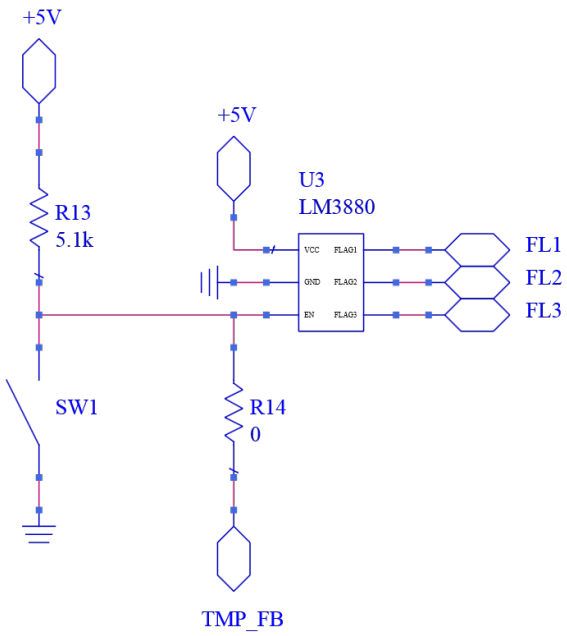


Figure 3 - Supply Sequencing Circuit

A mechanical SPST switch is used to control the state of the LM3880 logic input in nominal operation. Therefore, when the On/Off switch is in the "**off**" position, the open-drain flag lines are pulled low. When the On/Off switch is moved to the "**on**" position, the flag lines float high in order (FL1, FL2, FL3) over a 360ms time period (120ms between each flag).

Additionally, a provision has been made to pull the LM3880 logic input low from an external over-temperature alarm line, such as one provided by a thermostat device such as a Texas Instruments TMP709. The alarm line allows the user to incorporate a temperature IC located close to the target GaN FET RF device by making a connection via the ribbon-cable to the bias board, allowing for automatic shut down if the target device becomes too hot. A pin-by-pin description and important application information for the LM3880 can be found in the manufacturer's datasheet.

Gate Bias Supply Circuits

The application board is capable of biasing two GaN FET depletion mode devices, so two individual gate bias voltages are generated and applied.

When the On/Off switch is "**off**", both Gate voltages will be set to -4.35V. This is accomplished by pulling the adjust pin of the voltage regulator to ground through a 1kohm resistor (Flags FL2 or FL3 are driven low by the sequencing IC).

When the SPST switch is "**on**", both gate voltages are determined by their respective potentiometers. These have been pre-set before the board was shipped, but can be adjusted by turning the screw of the appropriate multi-turn 25kohm potentiometer. The potentiometers are labeled "1" and "2" to indicate with gate voltage (V_{gs1} or V_{gs2}) is being adjusted. Figure 4 shows the gate voltage reference circuit implemented on the GaN bias board.

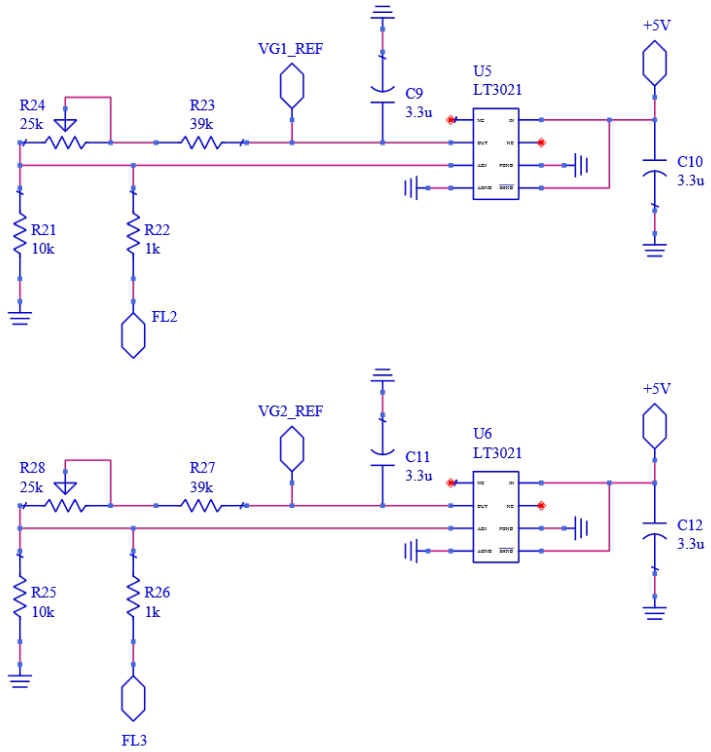


Figure 4 - Gate Voltage Reference Circuit

For a GaN FET device, gate current can flow in either direction, depending on the RF drive level of the FET. Therefore, any gate bias control circuit must be able to sink or source current. Additionally, the current drive level may be quite high for a high-power RF FET. For this reason, a high current dual op-amp was chosen to drive the two gate bias signals (V_{gs1} and V_{gs2}). Figure 5 shows the gate bias drive circuit implemented on the GaN bias board.

One additional note is that the LT1497 op-amp should have a series resistance between the output pin and any bulk capacitance that may be present on the gate feed line of the RF board. This resistor value should be in the 10-20 ohm range. The resistor is not shown on the schematic below because it has been implemented on the CDI designed GaN device evaluation board. *However, other GaN evaluation boards may not have such a resistor, so one should be added to keep the LT1497 from oscillating.*

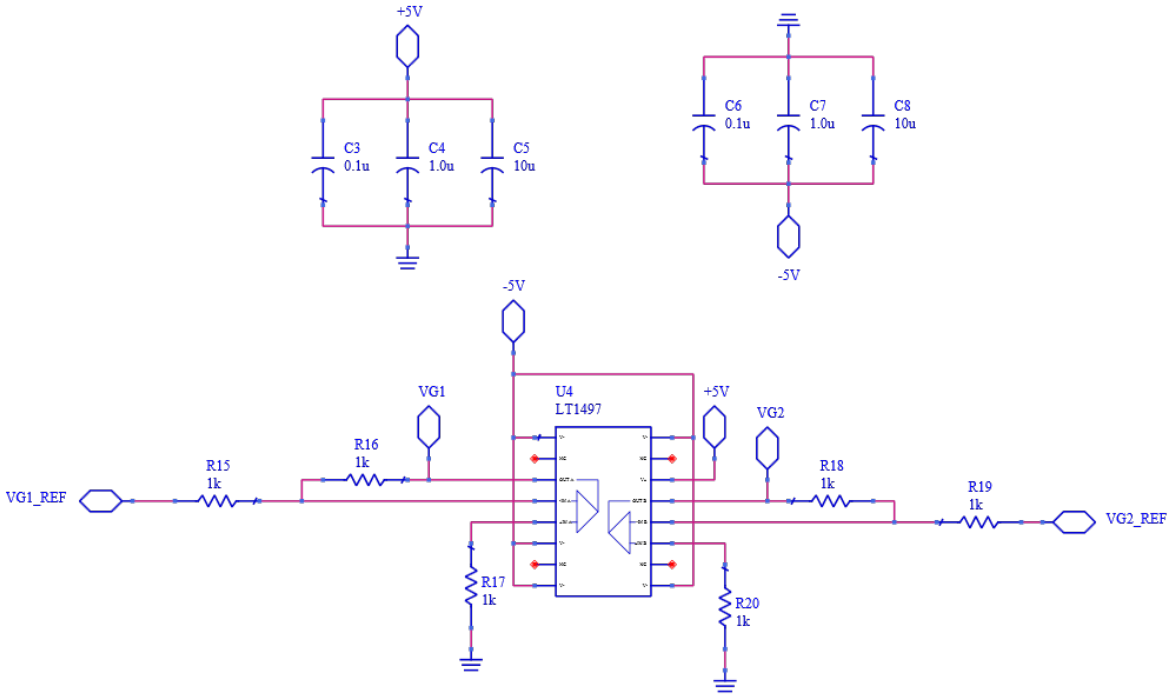


Figure 5 - Gate Voltage Driver Circuit

Drain Supply Current Control and Protection

The presence of both a +5V and -5V bias rail must be a pre-condition to enable a Linear Technology LT4256-1CS8 "Hot Swap" controller IC. This is accomplished using a pair of opto-isolators. These provide a safety mechanism that insures that both of these supply voltages are present before the Drain voltage can be enabled. The implementation is shown in Figure 6.

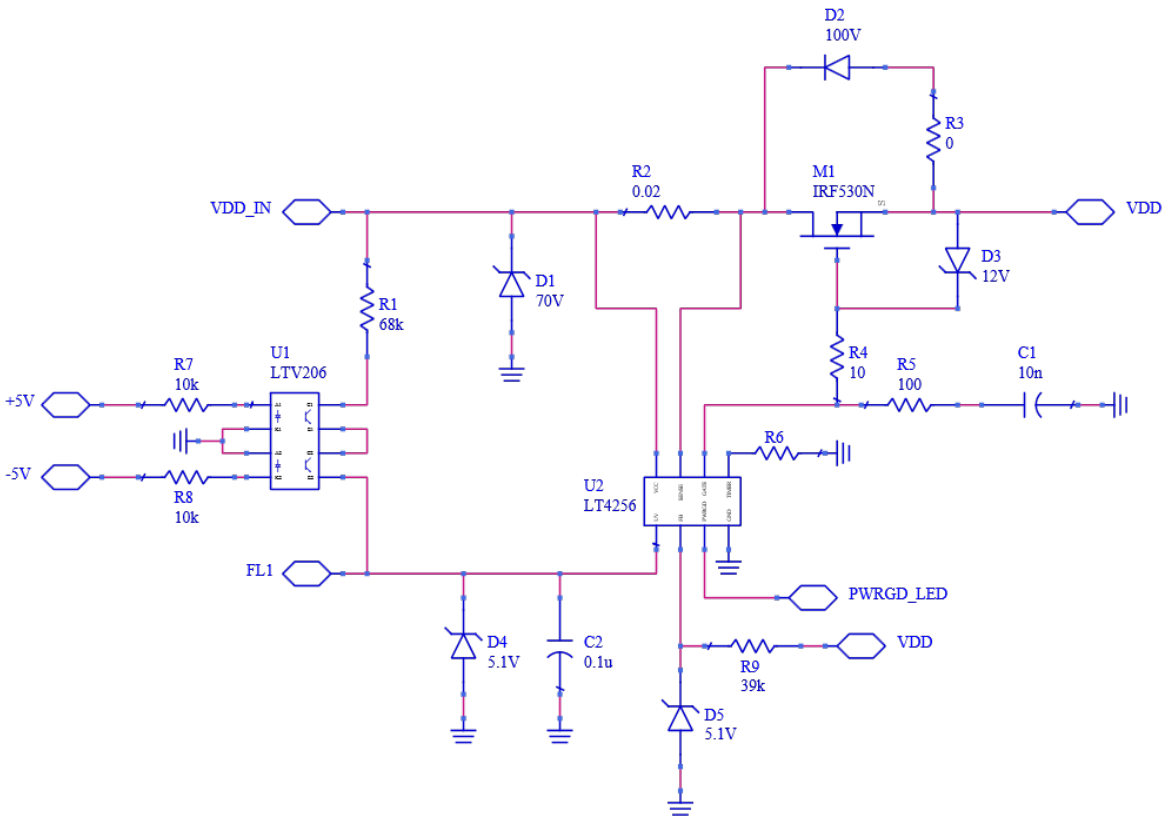


Figure 6 - Drain Control Circuit

To be "turned-on", the UV pin of the LT4256 must be > 4V. A 5.1V zener diode is used to regulate the voltage at the UV pin. The supply voltage for the zener diode comes from the 50V rail (V_{ds} rail) through the dual opto-isolator. The UV pin is also attached to the flag signal (FL1) from the sequencing IC. Therefore, 50V, +5V, -5V, and the On/Off switch must be in the "**on**" position for V_{ds} to be applied to the GaN device.

The LT4256 is used to drive an n-channel MOSFET that supplies voltage to the drain of the GaN FET. The V_{gs} voltage of the n-channel MOSFET is ramped up or down at a controlled rate by the LT4256. The LT4256 uses a current sense resistor that allows up to 2A to pass, but will shut-down the circuit should an over-current condition occur. This provides additional protection for the GaN RF transistor device. The current shut-down can be adjusted by changing the sense resistor. Refer to the LT4256 device datasheet for more details. *However, caution should be used in higher current configurations, as the n-channel MOSFET "on resistance" may cause excess heat. A different n-channel MOSFET may be required, depending on the amount of current being drawn, the duty cycle of that current, and the associated air flow and ambient temperature conditions.*

The LT4256-1CS8 also provides a signal when the drain voltage is fully on. This signal is used to drive a green LED on the circuit board. When the Green LED is lit, V_{ds} is "**on**".

LED Indicator

The application board uses a green LED to show when the drain bias voltage has been applied. This allows the engineer to determine at a glance if the GaN FET circuit bias is "**on**". *However, due to the off-state conditions of the LT4256-1CS8, the Green LED will also be lit if the +5V and -5V supplies are connected, but the 48V supply is not connected. This operational state is ok, since there is no voltage present on the drain of the GaN device.*

In normal operation, with all three lab supply voltages enabled, the green LED will be off when the drain voltage (V_{ds}) is "**off**" and the green LED will be on with the drain voltage is "**on**". The LED will also be off if there is a problem with either the +5V or -5V supply connections, as long as the 48V supply itself is still enabled.

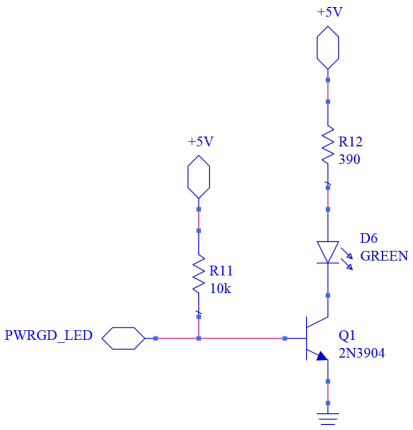


Figure 7 - LED Driver Circuit